

Notice of References Cited	Application/Control No. 09/982,061	Applicant(s)/Patent Under Reexamination MONROE, ERIC M.	
	Examiner Akash Saxena	Art Unit 2128	Page 1 of 2

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,260,998	07-2001	Garfinkel et al.	374/57
	B	US-6,188,582	02-2001	Peter, Geoffrey	361/760
	C	US-			
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	¹ "A Mechanism-Based Methodology for Processor Package Reliability Assessment", Nicholas P. Mencinger; Intel Technology Journal Q3, 2000; www.intel.com/technology/itj/q32000.htm
	V	² "Application Specific Semiconductor Device Qualification Methodology" by Matt Doty, Amkor, HDP User Group International, Inc; Nov 12 1998; http://www.hdpug.org/public/4-papers/1999/1999.htm
	W	³ "ReliaSoft's ALTA 1.0 - On Site Training Guide"; Realissoft Corporation; 1999; http://reliasoft.com/
	X	⁴ Semiconductor Device Reliability Failure Models", Ted Dellin et al; May 31 2000; SEMATECH Inc; Technology Transfer # 00053955A-XFR; http://www.sematech.org/docubase/document/3955axfr.pdf

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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